FIG. 1

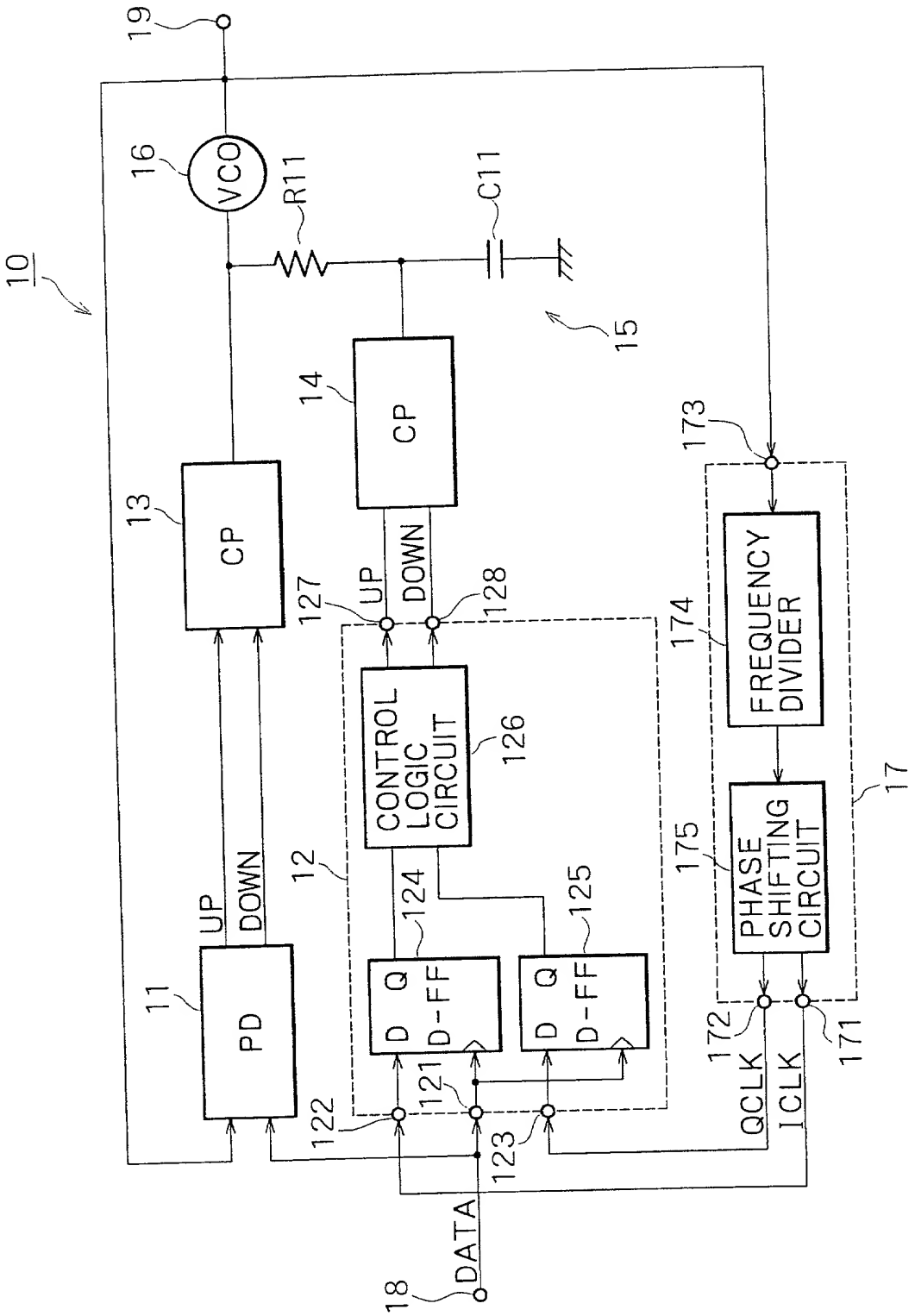

10
11
PD
UP
DOWN
12
13
CP
14
CP
15
16
VCO
R11
C11
17
18
DATA
19
121
122
123
124
125
D Q
D-FF
D Q
D-FF
126
CONTROL
LOGIC
CIRCUIT
127
UP
128
DOWN
171
172
QCLK
ICLK
173
174
FREQUENCY
DIVIDER
175
PHASE
SHIFTING
CIRCUIT

FIG.2

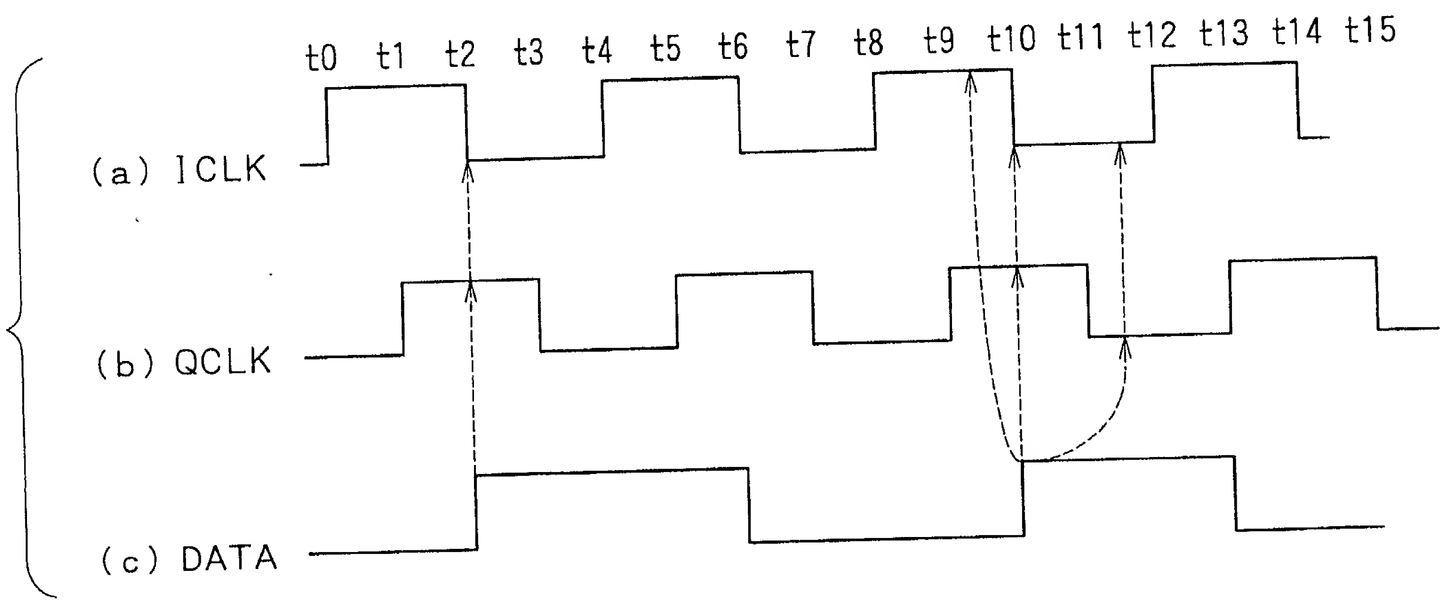

t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
(a) ICLK
(b) QCLK
(c) DATA

FIG. 3

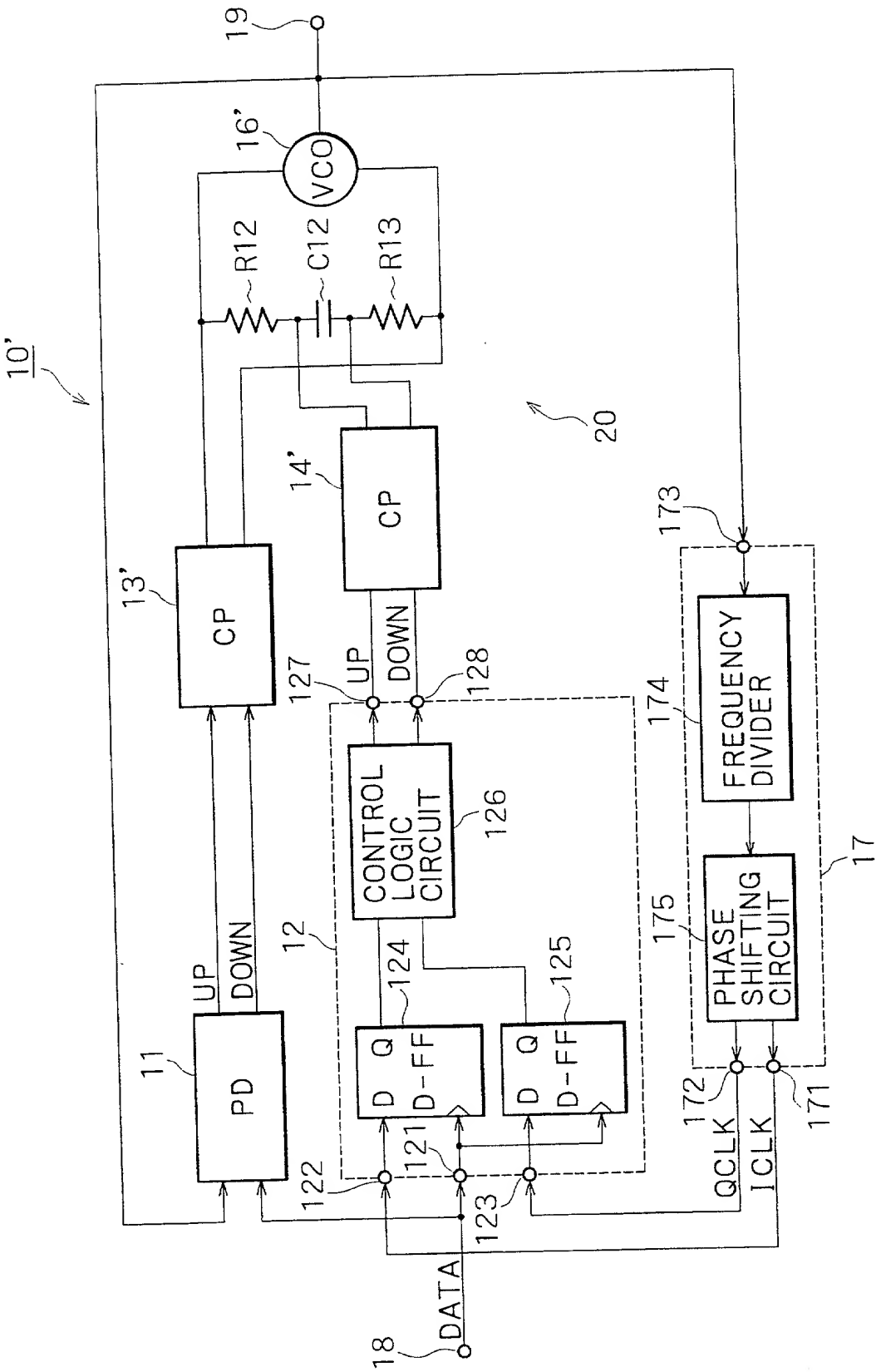

10'
19
16'
VCO
R12
C12
R13
20
14'
CP
13'
CP
173
FREQUENCY DIVIDER
174
127
UP
DOWN
128
CONTROL LOGIC CIRCUIT
126
12
124
125
175
PHASE SHIFTING CIRCUIT
17
11
PD
UP
DOWN
D Q
D-FF
D Q
D-FF
121
122
123
172
171
QCLK
ICLK
18
DATA

FIG.4

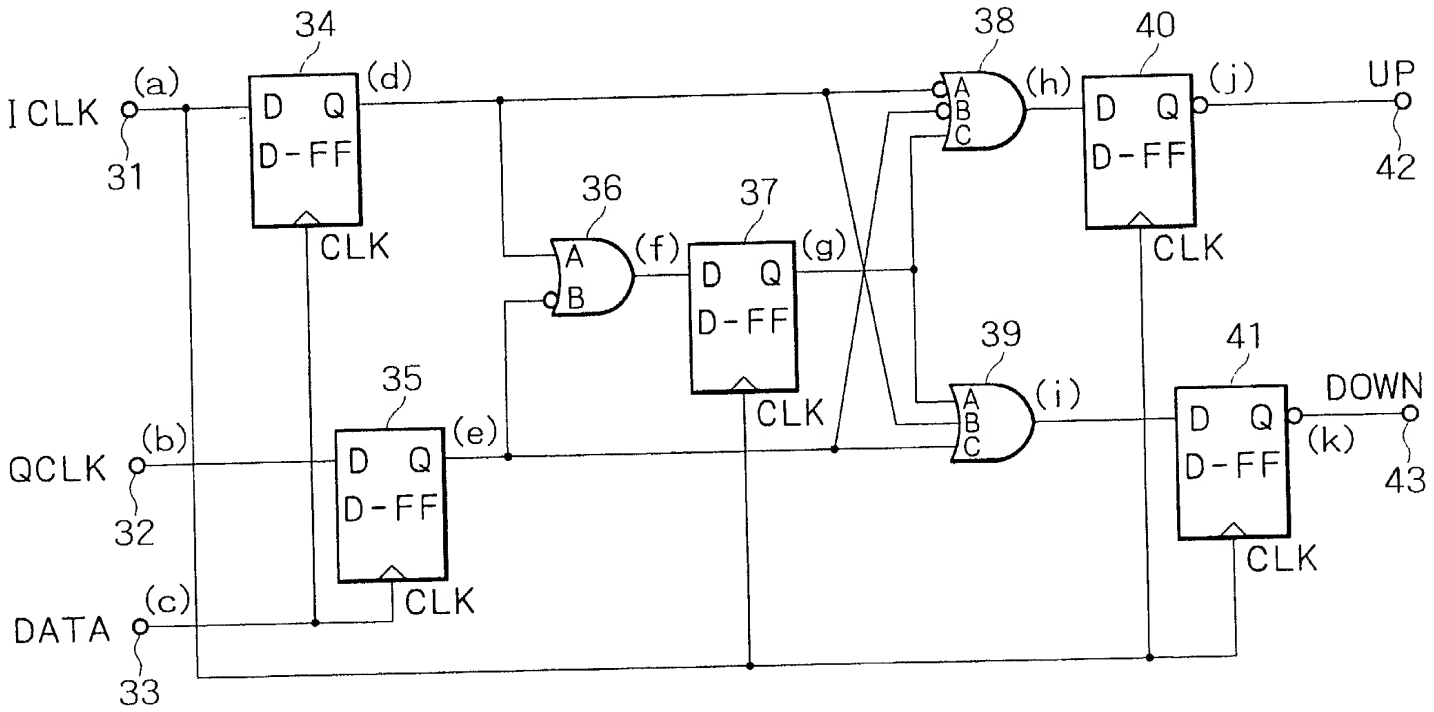

ICLK
(a)
31
34
D Q
D-FF
CLK
(d)
36
A
B
(f)
37
D Q
D-FF
CLK
(g)
38
A
B
C
(h)
40
D Q
D-FF
CLK
(j)
UP
42
QCLK
(b)
32
35
D Q
D-FF
CLK
(e)
39
A
B
C
(i)
41
D Q
D-FF
CLK
(k)
DOWN
43
DATA
(c)
33

FIG.5

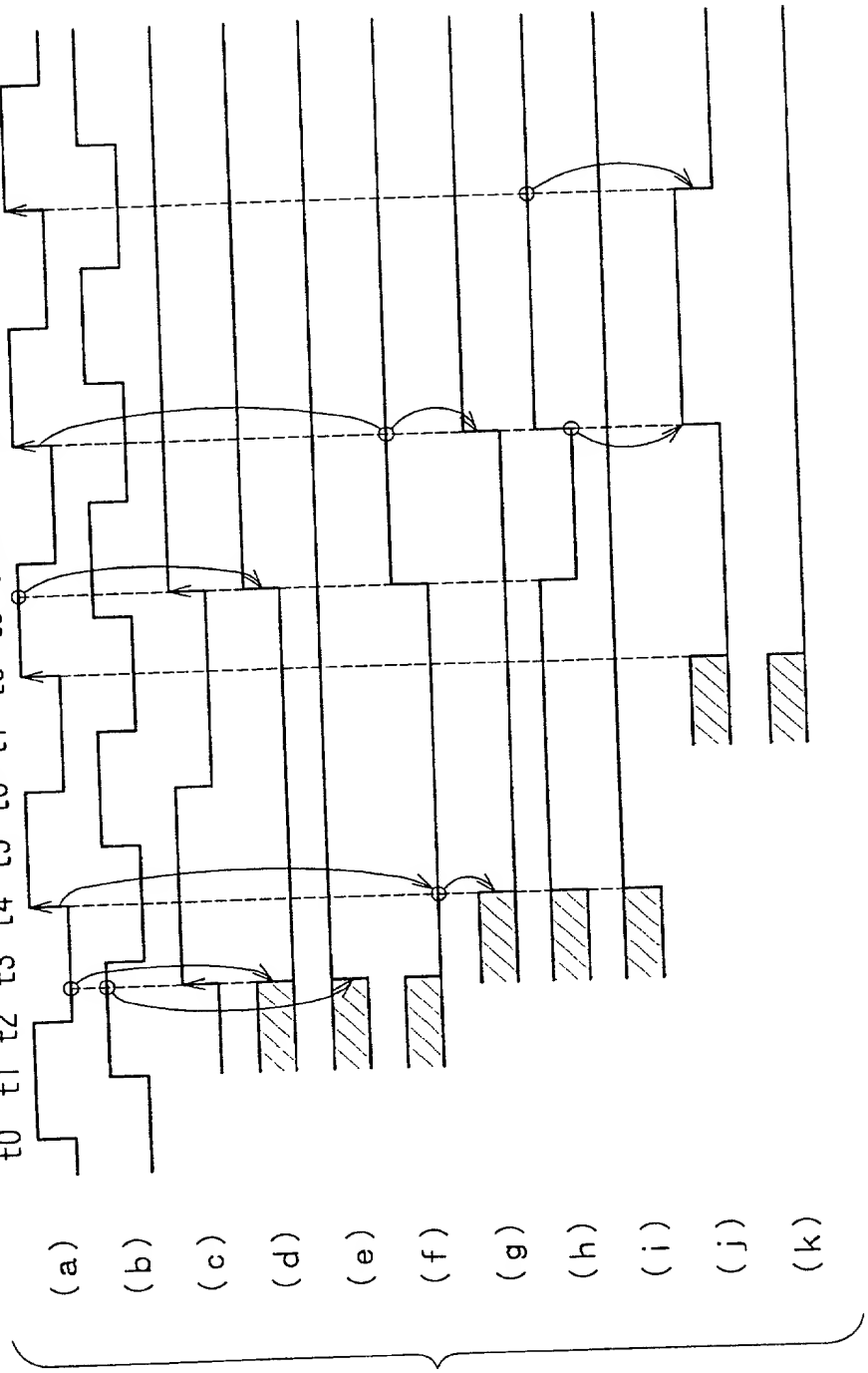

t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17 t18
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
(j)
(k)

FIG. 6

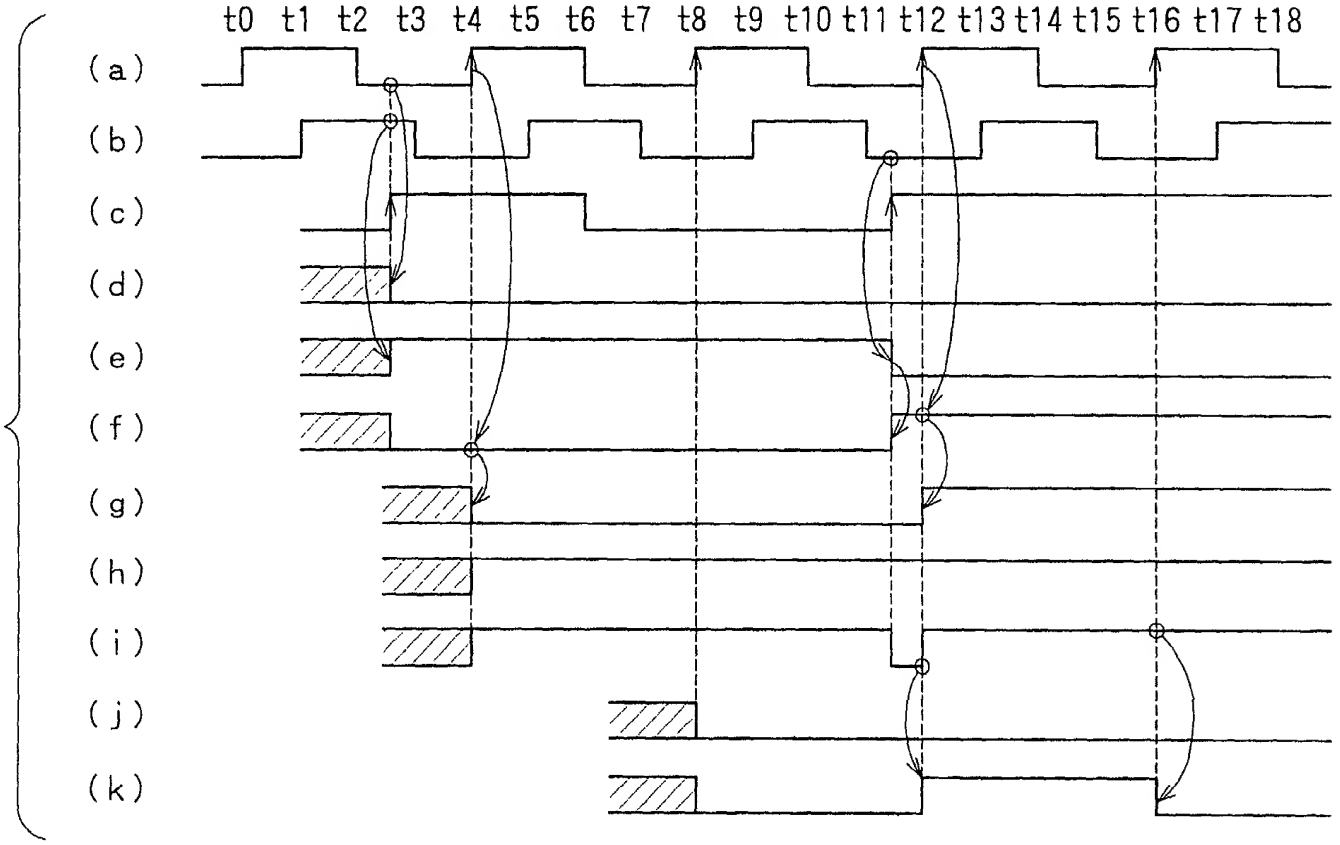

t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17 t18
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
(i)
(j)
(k)

FIG. 7

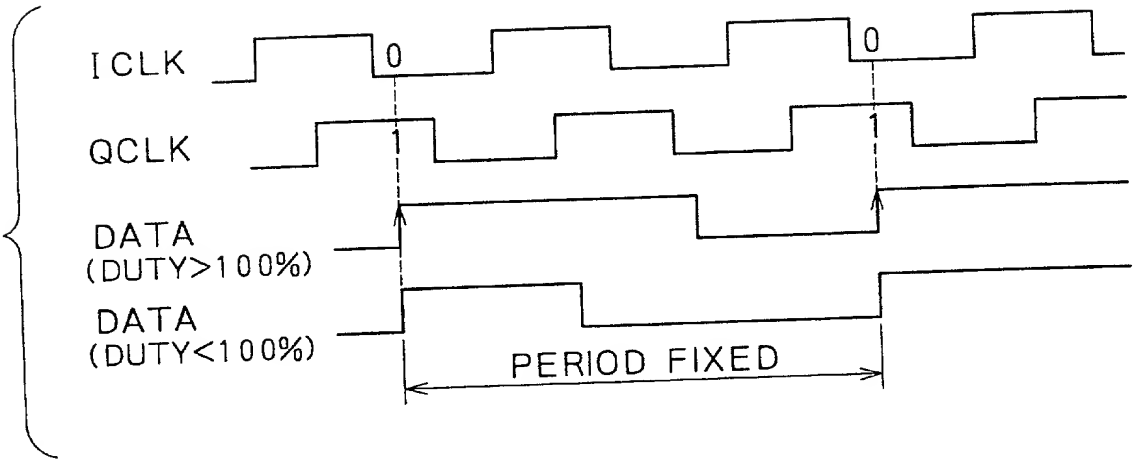

ICLK
QCLK
DATA
(DUTY>100%)
DATA
(DUTY<100%)
0
1
0
1
PERIOD FIXED

FIG. 8

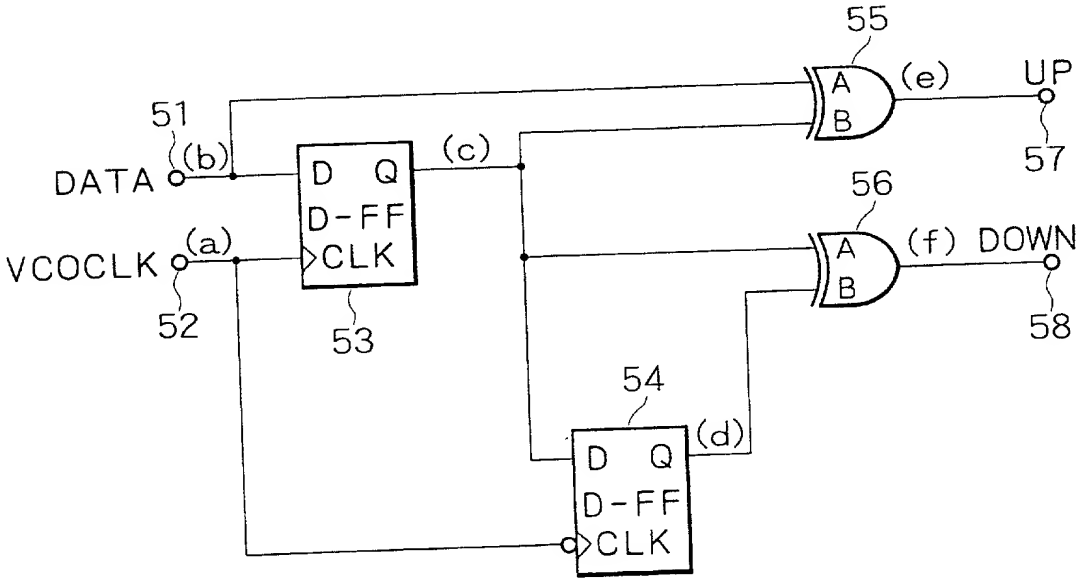

55
A
B
(e)
UP
57
51
(b)
DATA
D Q
D-FF
CLK
(c)
56
A
B
(f) DOWN
58
(a)
VCOCLK
52
53
54
D Q
D-FF
CLK
(d)

FIG. 9

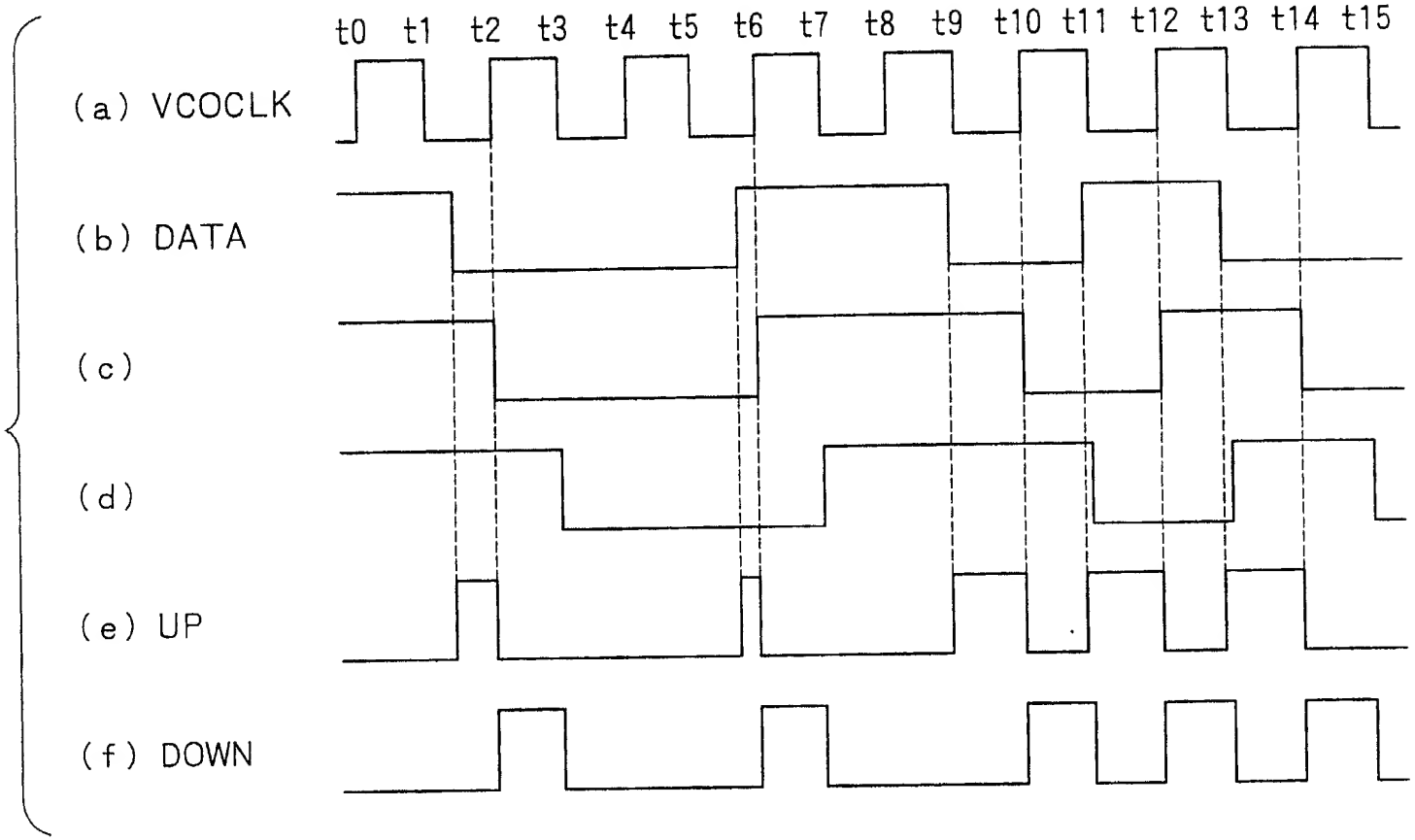

t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15
(a) VCOCLK
(b) DATA
(c)
(d)
(e) UP
(f) DOWN

FIG. 10

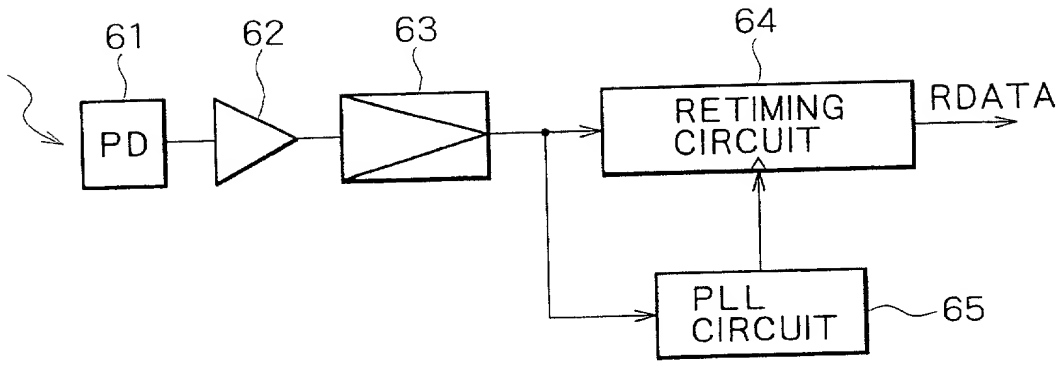

61
62
63
64
PD
RETIMING CIRCUIT
RDATA
PLL CIRCUIT
65

FIG. 11

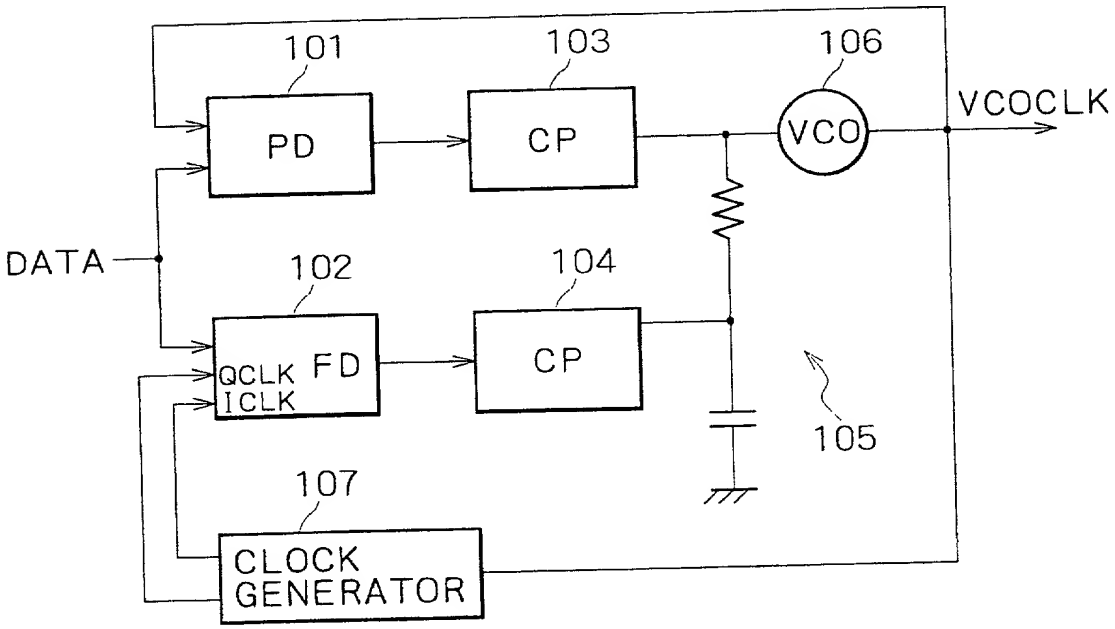
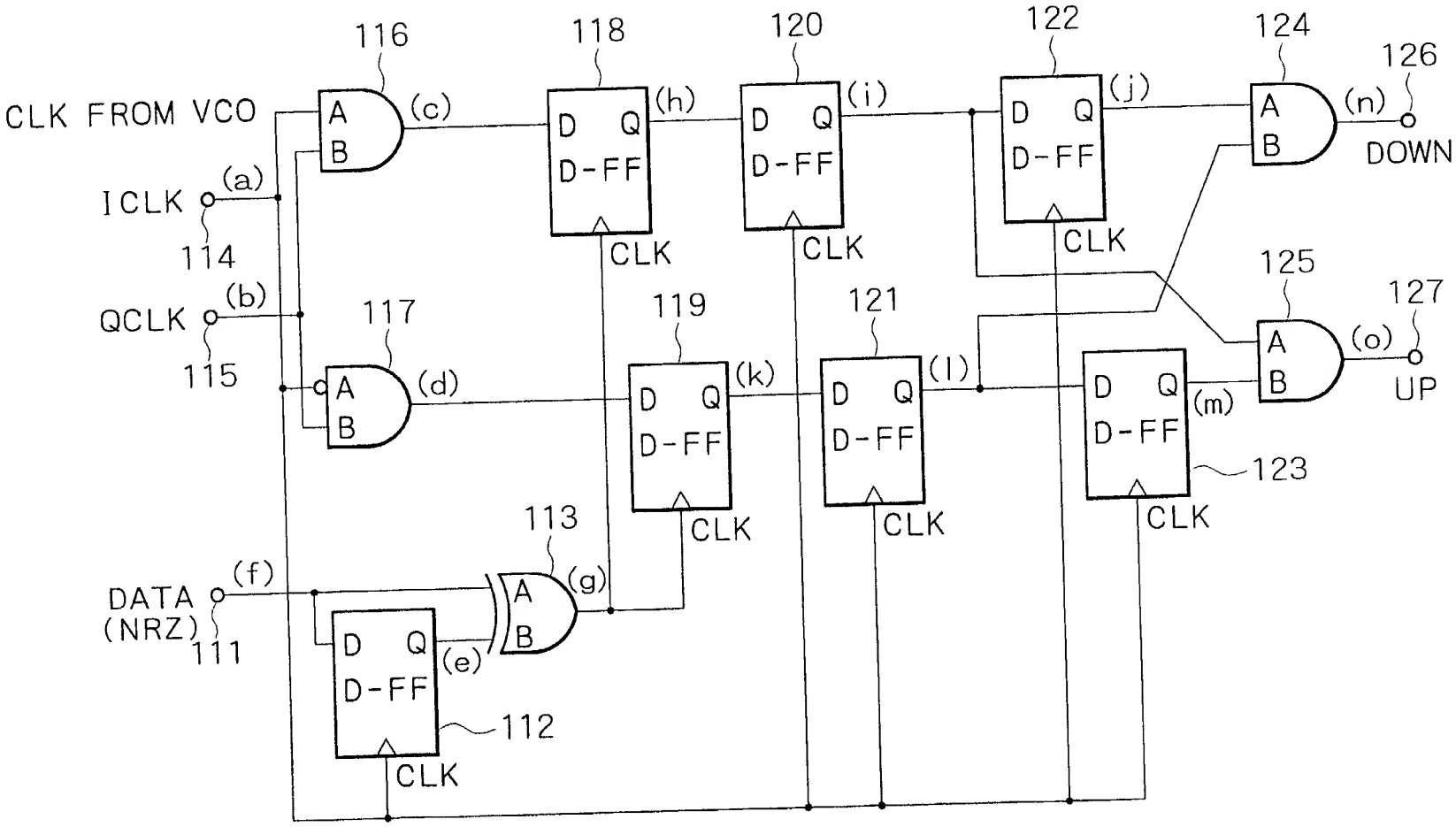

101
103
106
PD
CP
VCO
VCOCLK
DATA
102
104
QCLK FD
ICLK
CP
105
107
CLOCK GENERATOR

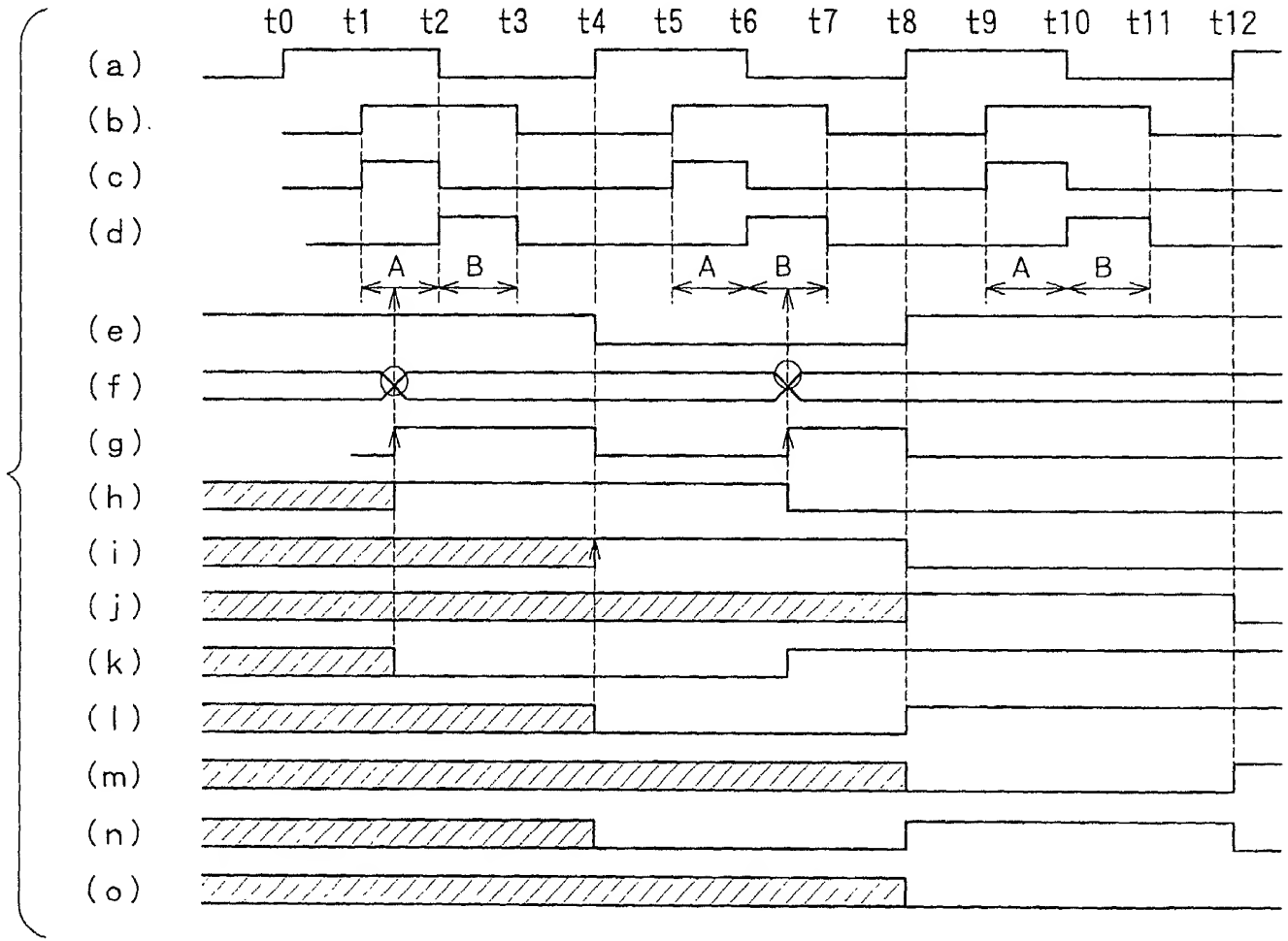
FIG. 12



ICLK : VCO OUTPUT CLK

QCLK : DELAYED BY 90° FROM ICLK

FIG. 13


t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
(a)
(b)
(c)
(d)
A
B
A
B
A
B
(e)
(f)
(g)
(h)
(i)
(j)
(k)
(l)
(m)
(n)
(o)

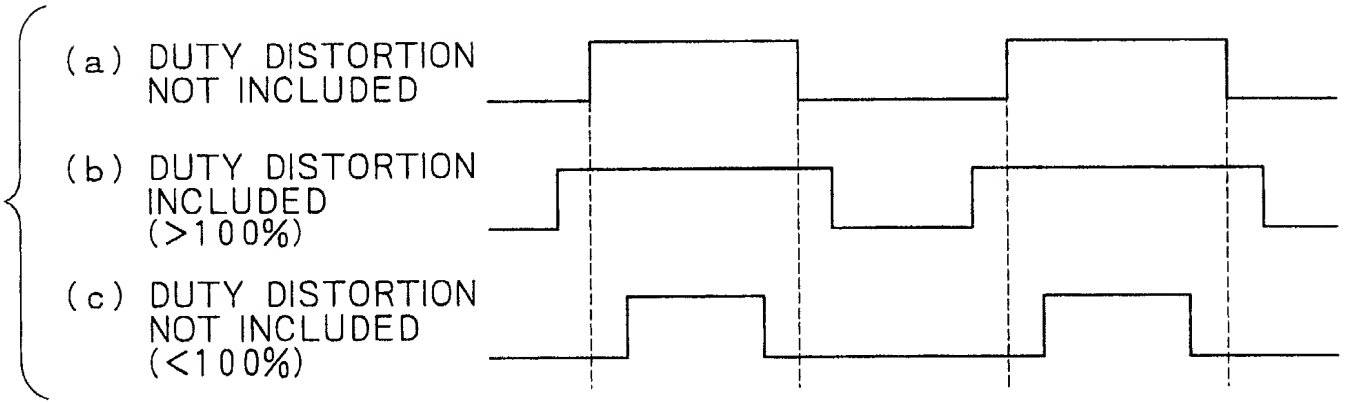
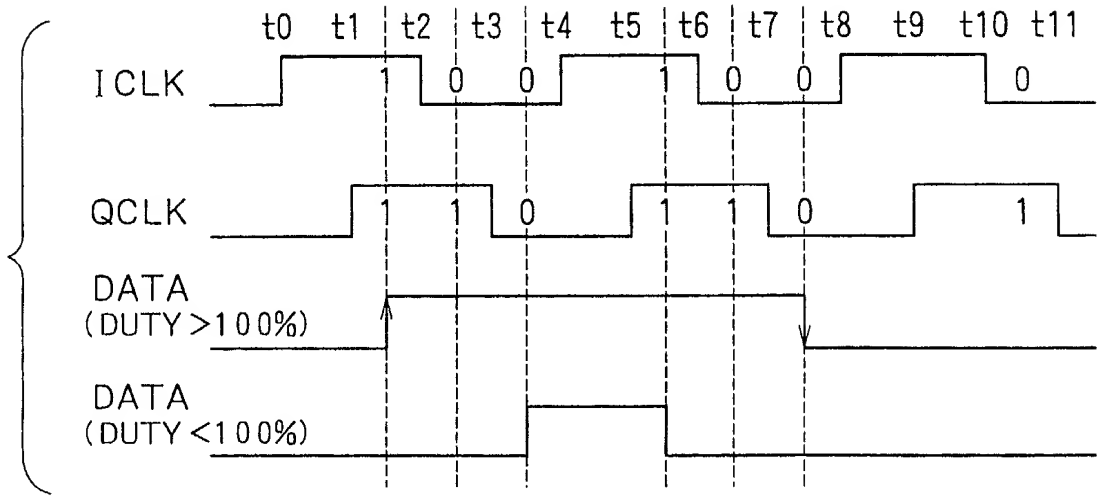

(a) DUTY DISTORTION NOT INCLUDED
(b) DUTY DISTORTION INCLUDED (>100%)
(c) DUTY DISTORTION NOT INCLUDED (<100%)

FIG. 15


t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11
ICLK
1 0 0 1 0 0 0
QCLK
1 1 0 1 1 0 1
DATA (DUTY>100%)
DATA (DUTY<100%)